TEXAS INSTRUMENTS

TLV2543EVM

User's Guide

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Mixed-Signal Products

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.3 V to 5.0 Vand the output voltage range of 0 V and 5.0 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

The purpose of this users guide is to serve as a reference manual for the TLV2543 12-bit analog-to-digital converter evaluation module (EVM). This document provides information to assist hardware and software engineers in application development.

How to Use This Manual

This document contains the following chapters and appendixes:
Chapter 1 – Overview
Chapter 2 – Hardware Description and Operation
Chapter 3 – Software Program and Flowcharts

Notational Conventions

- Program listings, program examples, and interactive displays are shown in a `special typeface` similar to a typewriter. Examples use a **`bold version`** of the special typeface for emphasis; interactive displays use a **`bold version`** of the special typeface to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

  Here is a sample program listing:

```
0011  0005  0001         .field    1, 2
0012  0005  0003         .field    3, 4
0013  0005  0006         .field    6, 3
0014  0006               .even
```

  Here is an example of a system prompt and a command that you might enter:

```
C:  csr –a /user/ti/simuboard/utilities
```

- In syntax descriptions, the instruction, command, or directive is in a **bold typeface** font and parameters are in an *italic typeface*. Portions of a syntax that are in **bold** should be entered as shown; portions of a syntax that are

in *italics* describe the type of information that should be entered. Here is an example of a directive syntax:

.asect "*section name***",** *address*

.asect is the directive. This directive has two parameters, indicated by *section name* and *address*. When you use .asect, the first parameter must be an actual section name, enclosed in double quotes; the second parameter must be an address.

- Square brackets (**[** and **]**) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets; you don't enter the brackets themselves. Here's an example of an instruction that has an optional parameter:

  LALK *16–bit constant [, shift]*

  The LALK instruction has two parameters. The first parameter, *16-bit constant*, is required. The second parameter, *shift*, is optional. As this syntax shows, if you use the optional second parameter, you must precede it with a comma.

  Square brackets are also used as part of the pathname specification for VMS pathnames; in this case, the brackets are actually part of the pathname (they are not optional).

- Braces ({ and }) indicate a list. The symbol **|** (read as *or*) separates items within the list. Here's an example of a list:

  ```
  { * | *+ | *– }
  ```

  This provides three choices: *, *+, or *–.

  Unless the list is enclosed in square brackets, you must choose one item from the list.

- Some directives can have a varying number of parameters. For example, the .byte directive can have up to 100 parameters. The syntax for this directive is:

  .byte $value_1$ *[, ... ,* $value_n$*]*

  This syntax shows that .byte must have at least one value parameter, but you have the option of supplying additional value parameters, separated by commas.

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

TLV2543C, TLV2543I 12-Bit Analog-to-digital Converters With Serial Control and 11 Analog Inputs data sheet (literature number SLAS096)

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Chapter 1

Overview

The TLV2543EVM evaluation module provides a platform for evaluating the TLV2543 analog-to-digital converter (ADC). For ease of evaluation, the ADC is interfaced with a microcontroller, three sensors, and a display. The onboard sensors provided are:

- An optical sensor
- A temperature sensor
- A variable resistor

Eight additional analog inputs are available for user-provided signals. Provisions are made for attaching these signal lines to a user-supplied connector. Terminals for an external power supply are also provided. This chapter includes the following topic:

Topic **Page**

1.1 Introduction

The TLV2543EVM consists of a TLV2543 12-bit ADC interfaced with a TSL250 optical sensor, a transistor based temperature sensor, a TL1431 voltage reference, a TLV2264 quad op-amp to provide 4 analog signal buffers, a TL7726 hex clamping circuit for signal over-voltage protection, a TMS370C712 microcontroller, three TIL311 hex display characters, and a TPS7233 3.3 volt regulator powering the TLV2543, TLC2264, 74LVC244A and the sensors.

The microcontroller reads the user-programmed dip switches and communicates with the TLV2543 to select the desired analog input, initiate the conversion process, and transfer the converted data back to the microcontroller. The microcontroller then transforms the data into hex form and transfers the result to the three TIL311 displays. A 74LVC244A octal buffer is used as a buffer between the microcontroller and the displays.

A TL7705 power supply voltage monitor resets the processor at power-on or if the power supply voltage drops below the proper operating level.

Jumper provisions are made to connect the TLV2543 reference voltage to 3.3-V power for ratiometric measurements or to an absolute voltage provided by a TL1431 voltage reference device.

A connector pattern is provided for the user to install an interface connector. An uncommitted breadboard area is also provided. An external 5-V power supply (4.75 V to 5.25 V at 0.5 A) is required for operation.

Chapter 2

Hardware Description and Operation

This chapter contains descriptions of the hardware and operation of the TLV2543EVM. This chapter includes the following topics:

Topic **Page**

2.1 Setup and Operation

The power supply terminals (J2) on the TLV2543 EVM module must be connected to a regulated 4.75-V to 5.25-V power supply capable of providing at least 0.5 A.

This evaluation module is designed to have power supplied from an external regulated 5-V power supply. No form of power supply regulation is included on the module. Damage to the components can and will occur if the voltage exceeds the maximum specified level. Under voltage can cause improper operation.

When the power supply is switched on, the microcontroller is initialized and the displays flash to indicate proper operation. The displays then show a two or three digit hex value of the voltage generated by the optical sensor and digitized by the TLV2543. The value on the displays varies with the intensity of the light striking the TSL250 sensor (See the *Optical Sensor* section).

The input select switch (S1) is set to the hex address (LSB on the right) which selects the desired TLV2543 input (See the *Input Select Switch* section). The desired A/D converter reference voltage for a given sensor is selected by moving the Ref Select jumper (JP9) to the onboard reference (REF V) position or the power supply (V_{CC}) position.

The TLV2543EVM is shipped with the settings listed in the following table:

Table 2–1. EVM Default Settings

Function	Setting
Input select switch (S1)	0000 hex (optical sensor selected)
Reference select jumper (JP9)	REF V
Input jumpers (JP1, JP2, JP3, JP11, JP12)	Ground
Output jumpers (JP4, JP5, JP6, JP7, JP8)	Shorted
Ref– jumper (JP10)	Shorted

NOTE: The input and output jumpers and the REF– jumper on the TLV2543EVM are formed by a top side copper trace on the PC board between two plated through holes. If desired, the trace can be carefully cut to remove the jumper. The two through holes allow the user to restore the jumper with a wire or connector.

A hole pattern is provided for a user-supplied connector to allow easy application of external analog signals for additional evaluation (See the *Interface Connector Provisions* section).

The following sections give more specific information about each selected sensor input and selected reference.

2.2 Input Select Switch

The four position dip switch (S1) labeled input select allows the user to select the desired analog input of the TLV2543. The switch is treated as a hex address command (MSB on left, LSB on right) as listed in the following table:

Table 2–2. Input Select Switch Descriptions

Hex	Binary	Function Selected	Typical Response
0h	0000	Optical sensor input	User controlled light intensity
1h	0001	Temperature sensor input	588h + temperature change
2h	0010	Potentiometer input	User adjusted
3h	0011	IN3 buffer input	000h or user input
4h	0100	IN4 buffer input	000h or user input
5h	0101	IN5 buffer input	000h or user input
6h–Ah	0110–1010	IN6 through IN10 inputs	000h or user input
Bh	1011	(V_{ref} input)/2 test	800h
Ch	1100	–V_{ref} input (ground) test	000h
Dh	1101	V_{ref} input test	FFFh
Eh	1110	Enter power down mode	Display blank
Fh	1111	Fast conversion rate on IN4 input	User input

Note: Inputs IN3 through IN10 are made available to a user supplied connector (see the *Interface Connector Provisions* section).

2.3 Microcontroller

The TMS370C712 microcontroller (U4) samples the status of the input select switch on ports A4 through A7. This sample data, which is sent to the TLV2543 through the serial peripheral interface ports SPICLK, SPISIM0, and SPISOM1, determines which specific multiplexer input is converted. The microcontroller then reads back the converted 12 bits and changes the data into three hexidecimal digit values. The hexidecimal data is transferred to the three hexidecimal displays U7, U8, and U9. Five sections of the 74LVC244A octal buffer are used to drive the common bused TTL inputs of the displays.

For all input select positions except Fh, the microcontroller instructs the TLV2543 to perform the analog-to-digital conversions and display the results at a rate of approximately 2 conversions per second. When the Input Select position is Fh, the microcontroller selects input IN4 and the conversions from the TLV2543 are at a rate of approximately 30k conversions per second (See the *Fast Conversion Rate* section).

NOTE: The following information applies to the TMS370C712 serial peripheral interface (SPI) to the TLV2543.

The TLV2543 strobes in the command data bits from the microcontroller on the DIN port at the rising edge of the clock pulse on the I/O CLK terminal. The TMS370C712 generates a clock rising edge on the SPICLK port and also at that time, while conforming to the SPI interface requirements, the data output on the SPISIM0 port changes to reflect the next serial bit to be transferred.

If the SPICLK output is connected directly to the TLV2543 I/O CLK input, the required data setup time for the data to be present before a rising clock edge is applied cannot be less than 100 ns (see the *TLV2543* data sheet). To solve this race condition, a resistor (R24) and capacitor (C21) provide a delay to the rising clock edge. One buffer section of the 74LVC244A octal buffer (U6) is used to buffer the delayed clock signal. If only one TLV2543 is being used (as with this EVM), the buffer is not normally required. If several TLV2543 devices are being driven in a bus configuration, using this buffer is advised.

2.4 Power Supply Supervisor

Power supply voltage is monitored by the TL7705 (U5). When power is first applied, a microprocessor reset is held until the power supply voltage exceeds 4.55 V (nominal). The reset is then released and the microprocessor begins operation.

During normal operation, if the power supply voltage falls below 4.55 V, a reset is activated again.

2.5 Optical Sensor

The TSL250 (U1) optical sensor is connected to the AIN0 multiplexer analog input port of the TLV2543. This sensor converts light intensity to an output voltage ranging from less than 10 mV (dark) to about 2 V (at 2 mW/sq cm illumination intensity).

The output of the optical sensor can be varied by placing an object such as a dark colored plastic marker pen cap over the sensor.

A practical application such as sorting can be demonstrated by holding similar objects of differing shades within the optical viewing range of the sensor (under a uniform intensity light) and noting the displayed values. A simple optical hood to mask ambient light (e.g. drill a hole in the side of the marker pen cap) provides more uniform results.

NOTE: Office light generated by typical artificial lighting contains a high component of ac line frequency intensity variations not normally perceived by the human eye. These variations are detected by the optical sensor. Since the ADC is commanded to make measurements at random times with respect to the ac line frequency, the converted values appear to be unstable in the lower order bits, even though each individual measurement is accurate. This line frequency light intensity variation can be minimized by using dc power to drive the dominate light source (light emitting diodes work well) in addition to shielding the sensor from the ac driven room lighting.

An extension of the sorting concept can yield a simple color sorting sensor system. This system requires three optical sensors, each masked by a red, blue, or green optical filter. The individual readings from the three sensors can then be calibrated to the specific color of the object to be identified. For repeatable results, the intensity and color content of the illuminating light source must be uniform.

2.6 Temperature Sensor

When a single transistor and the 12-bit A/D conversion range of the TLV2543 are used, the following characteristics can be seen:

- A simple temperature sensor
- The textbook temperature variation of a transistor base-emitter junction
- The dc temperature instability of a simple one-transistor amplifier

The 2N2222A transistor (Q1) is connected in a classical feedback amplifier configuration that forces the collector voltage to a base-emitter junction voltage of 2 V_{be}. The base-emitter junction (essentially a forward biased diode) voltage is about 0.7 V at room temperature (25C°) and has a temperature variation of about –2.2 mV/C°. Therefore at room temperature, the collector voltage is approximately 1.4 V with a decrease of approximately 4.4 mV for each degree of temperature increase.

If the REF select jumper is set to the on-board reference (REF V) position, the conversion reference is set to approximately 2500 mV or 2.5 V. This setting allows the display to decrement approximately 1.6 counts for each mV or about 7 counts per C° of temperature increase.

If the ambient room temperature is approximately 25C° and human body temperature is approximately 38C°, the display should reduce about 91 counts when the transistor is held firmly between two fingers. For a more exact analysis, exact transistor characteristics, absolute reference voltage levels, exact room and finger temperatures, etc. would have to be taken into account.

2.7 Voltage Variable Input (Potentiometer)

The IN2 input is controlled by a potentiometer (R13). One section of the TLC2264 (U2) serves as a buffer amplifier for the AIN2 TLV2543 input port. When the potentiometer is adjusted over its range, the input voltage changes from 0 to $V_{CC}/2$ (approximately 3.3 V/2 = 1.65 V). Since the buffer amplifier has a gain of 2, the input to the TLV2543 port varies from 0 to V_{CC}.

For ratiometric measurements, the REF select jumper should be set to the V_{CC} position. Then the TLV2543 reference becomes V_{CC} and all A/D conversions are made relative to the value of V_{CC}. The potentiometer output voltage, by its connection, is also relative to V_{CC}. An A/D conversion of that voltage yields a value proportional to the setting of the potentiometer and independent of the power supply voltage.

2.8 Buffered User Inputs

The IN3 input is connected to the TLV2543 input port through unity gain configured buffer amplifiers (one section of the TLC2264, U2). Although providing unity gain (gain = +1), the input signal can only be within approximately 1.5 V (see the common mode input voltage range specifications of the TLC2264) of the power supply voltage to maintain predictable operation. As long as the power supply voltage to the TLC2264 remains at 3.3 V, this restricts the usable signal input voltage range from 0 V to 1.8 V, however this range can be acceptable for some input level requirements.

The input impedance is dictated by the 10 kΩ value of resistor R14 and can be changed to almost any suitable value due to the extremely high input impedance of the TLC2264.

Inputs IN4 and IN5 are connected to the TLV2543 input ports, each through a buffer stage of the TLC2264, and each with a gain of 2. The full output voltage swing of 0 V to 3.5 V to the ADC inputs is achieved with signal inputs of 0 V to 1.65 V as listed in Table 2–3.

Table 2–3. Buffered User Input Descriptions

Input	Gain	Unbuffered	Input Range
IN3	×1	N	0 V – 1.8 V (input to ADC is 1.8/3.3 of full scale)
IN4	×2	N	0 V – 1.65 V
IN5	×2	N	0 V – 1.65 V
IN6		Y	0 V – 3.3 V
IN7		Y	0 V – 3.3 V
IN8		Y	0 V – 3.3 V
IN9		Y	0 V – 3.3 V
IN10		Y	0 V – 3.3 V

2.9 Unbuffered Inputs

The IN6 through IN10 inputs are connected to ground by the top side circuit board etch jumpers JP1, JP2, JP3, JP12, and JP11, respectively. Any etch jumper can be removed by carefully cutting the copper trace between the feed-through holes at the JP marking, allowing that input to be connected to an external signal.

When these unbuffered inputs are used, the required TLV2543 specifications such as a low source impedance (see the *Driving the Input of a Switched Cpacitor ADC* section) and input voltage range (0 V to 3.3 V) must be used. The signal grounds should not be improperly connected to the high current power supply grounds (see the *Grounding Considerations* section).

2.10 Reference Select

The REF select jumper is provided to allow ratiometric measurements (jumper set to V_{CC}) or allow absolute measurements (jumper set to REF V) relative to a voltage reference established by the TL1431 (D1). This voltage reference is approximately 2.5 V.

Ratiometric measurements are made relative to the 3.3-V power supply voltage. If a sensor or input signal voltage is used that varies proportional to the 3.3-V power supply voltage (such as the potentiometer R13), then the signal becomes a ratio of the absolute value of the power supply voltage. Then, if the reference voltage is connected to 3.3 V (REF SELECT jumper position at V_{CC}), the TLV2543 tracks the power supply voltage and provides a converted result independent of the power supply voltage variations.

Absolute measurements are required if the sensor or input analog signal does not change with the power supply voltage. The previously described optical and temperature sensors are in this category. For these sensors, the REF select jumper is set to the REF V position.

2.11 Fast Conversion Rate

When the input select switch is set to Fh, the EVM module operates in a fast conversion rate mode. In this mode, the conversion rate is approximately 30k conversions per second from the IN4 input. The displays are updated once every 20 conversions.

2.12 Input Voltage Clamp

The TL7726 (VZ1) is connected to inputs IN3 through IN8. The TL7726 clamps an input signal voltage in excess of the power supply voltage level to prevent damage to the semiconductor inputs. Signal voltages below 0 V (ground) are clamped to ground. Signal inputs between 3.3 V and ground are not affected. The TL7726 provides protection for inputs from incidental transients due to static discharge, excessive signals, etc. Transient current protection is limited to 25 mA.

2.13 Interface Connector Provisions

A hole pattern for a user-supplied interface connector is provided at J1. A standard 8 × 2 set of header posts (such as an AMP 87215-5 or Molex 10-89-1161) can be soldered in place. This arrangement allows several different styles of connector to be installed as necessary to satisfy user requirements.

Figure 2–1. Interface Connector Hole Pattern

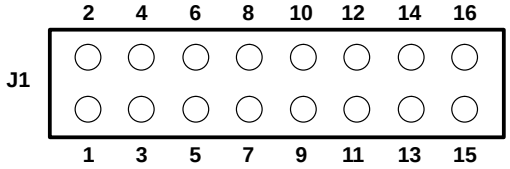


Table 2–4. Interface Connector Hole Pattern Descriptions

Hole	Circuit Function
1	NC
2	NC
3	IN3 input (buffered with +1X gain)
4	IN4 input (buffered with +2X gain)
5	IN5 input (buffered with +2X gain)
6	IN6 input
7	IN7 input
8	IN8 input
9	IN9 input
10	IN10 input
11	5 V
12	Signal ground
13	5 V
14	Power ground
15	5 V
16	Power ground

Note: Hole 12 can be used as a signal ground return to avoid the higher current ground return paths that are associated with a power supply ground.

2.14 Grounding Considerations

When designing analog circuits that share a ground with digital and high current power supplies, the voltage drop along the high current paths must be taken into account. This voltage drop is a result of the current flowing through the greater-than-zero resistance of the current path, and/or high frequency current transients flowing through the greater-than-zero inductance of a current path.

If the signal ground is connected to the power supply ground at the improper location, this voltage drop is injected into the signal ground and appears as part of the signal, causing an error.

The solution is to establish a single ground point on the PC board and connect all grounds individually to that point (the EVM single ground point is at the GND terminal of the power supply connector). By using this method, currents flowing along any one path to ground do not inject error voltages in any other ground path.

As a practical implementation, however, it may not be reasonable to run a separate ground trace for each component that connects to ground. Therefore, the next best approach is to group the higher current grounds (such as the power supply and digital grounds) together and run them to the central PC board ground point, while still maintaining separate ground paths for the analog grounds.

An analysis of current flow paths within the analog section will give an indication of which grounded components could be lumped together into a common ground path and which should be kept separate. For instance, on the EVM, it would be reasonable to use a common path for the TLV2543 REF– terminal and the TL1431 anode. This is because the only significant current flow is through the TL1431 (only about 1 mA) and is not enough to cause a significant error. A 1/2 LSB error at a reference voltage of 2.5 V would be about 0.3 mV, so the ground trace would have to be in excess of 0.3 Ω to cause such an error.

If all of the input signals are low current, such as the optical sensor (about 2 mA), the temperature sensor (about 1 mA) and the potentiometer (about 0.25 mA), it may be reasonable to use a common ground trace. As always, wider trace widths are desirable to keep the resistance low. If high currents are associated with any input signal, always use a separate PC board trace directly to the central ground point location.

Even though the operating current of the TLV2543 is low (2.5 mA max), some high speed current transients due to the internal digital switching are present and a separate ground trace is reasonable.

Note:

Always keep the power supply decoupling capacitor as close as possible to the supply pins. This means that the separate ground trace would actually be for the decoupling capacitor and the TLV2543 ground pin.

If free area is available, or if the PC board is multilayer, a large ground plane may be acceptable to connect all the analog side ground connections providing that any one signal ground connection is not carrying a large current. That ground plane should be connected directly to the central ground point without touching any of the digital or power supply ground locations along its path.

Treating the distribution of the digital and analog 5-V and 3.3 V current paths on the PC board in a similar manner to the grounds is also a good practice. The designated central power point location is the 5-V terminal of the power supply connector (J2) on the EVM board.

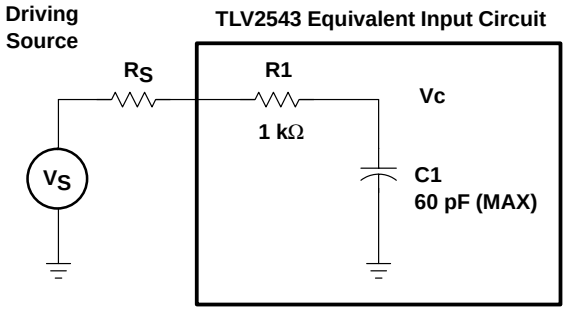
2.15 Driving the Input of a Switched Capacitor ADC

When applying an analog signal to the input of a switched capacitor ADC such as the TLV2543, care must be taken to provide a low enough impedance to the input terminal to charge the internal capacitor enough for an accurate conversion during the sampling phase of the converter. The sampling time will depend on the period of the I/O clock rate being used to drive the converter and the number of transfer bits commanded. With the maximum I/O clock frequency of 4.1 MHz and a 12-bit transfer mode, the TLV2543 uses 8 clock cycles (or about 2 μs) for the sampling time.

The input equivalent circuit of the TLV2543 looks like a series resistance and a capacitor to ground during sampling and an open circuit during conversion.

For accurate operation the input capacitor must be charged to the required accuracy of 1/2 LSB (or more, depending on the required system error budget) during the sampling phase of the ADC cycle.

Figure 2–2. Equivalent Input Circuit



The voltage on capacitor C1 is given by:

$$Vc = Vs\left(1–e^{-t/TC}\right) \quad (1)$$

Where TC is the time constant C1(Rs+R1)

The final voltage value of Vc within 1/2 LSB of Vs is

$$Vc\ (1/2\ LSB) = Vs - Vs/2^{n+1} \quad (2)$$

Where n is the resolution of the converter.

So equating equation 1 to equation 2 then

$$Vs - Vs/2^{n+1} = Vs\left(1 - e^{-t/TC}\right)$$

therefore the charging time in terms of the circuit time constants is

$$t\ (1/2\ LSB) = TC\ln\left(2^{n+1}\right)$$

For a 12-bit converter this would be:

t_S = TC x ln(8192) = 9 TC

The internal capacitance for the TLV2543 is 60 pF max and the internal series resistance is 1 KΩ. Therefore, with an I/O clock at 4.1 MHz, and a 12-bit transfer mode (sample period = 2 μs), the time constant should be no more than:

$$1/9 \times 2\ \mu s = 0.22\ \mu s$$

Therefore

$$C1(Rs+R1) = 0.22\ \mu s$$

So

$$(Rs+R1) = 3.67\ K\Omega$$

Since Rs = 1K, then the source impedance should be less than 2.67 KΩ to stay within 1/2 LSB error. Good design practice dictates that the source impedance be as low as possible, such as the output of an op-amp. However in an application where fast conversion time is not critical, slow I/O clock rates can allow the driving source impedance to be relatively large.

2.16 Board Schematic

The schematic of the EVM is shown in the following figure.

Figure 2–3. Board Schematic

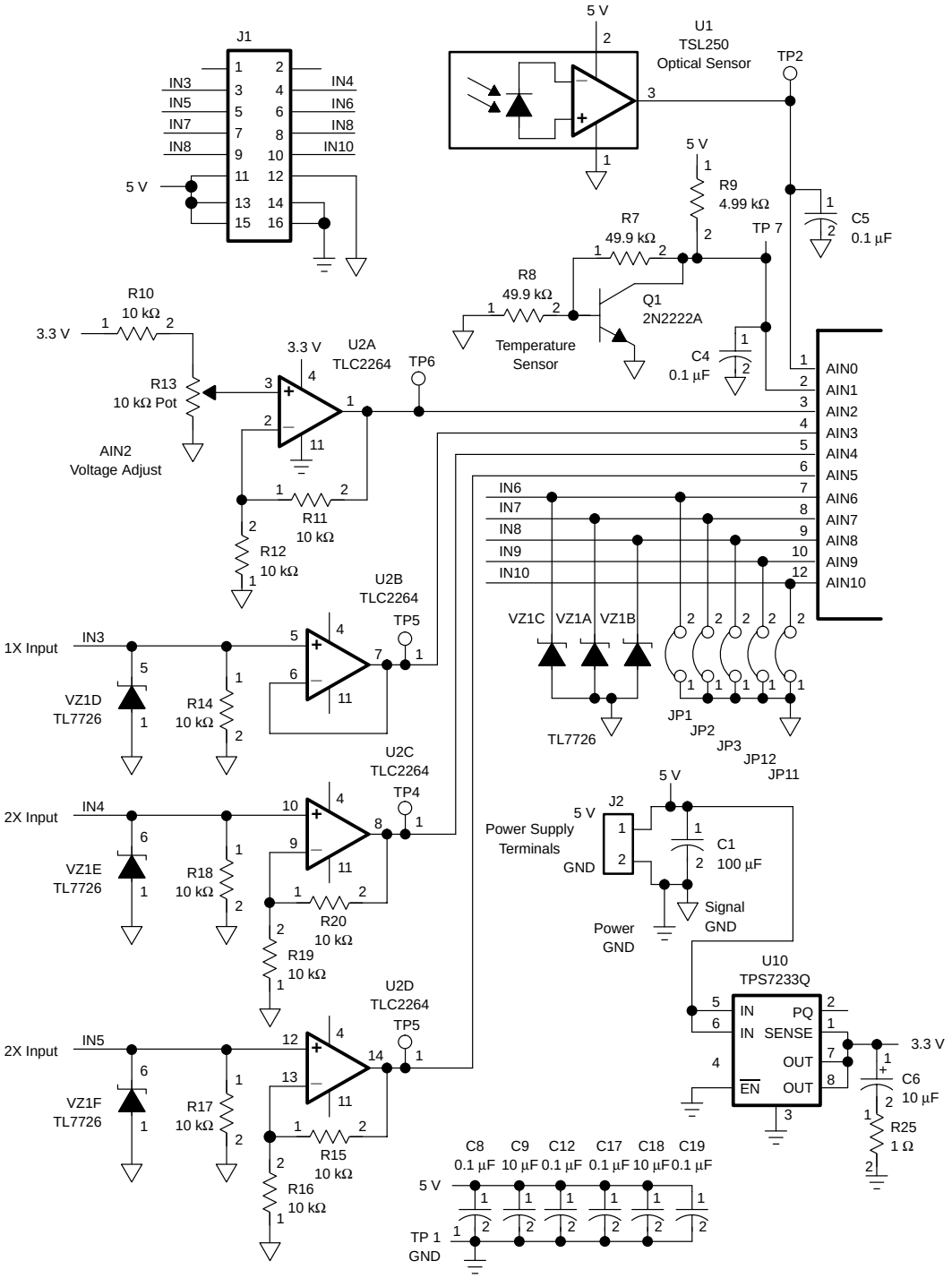
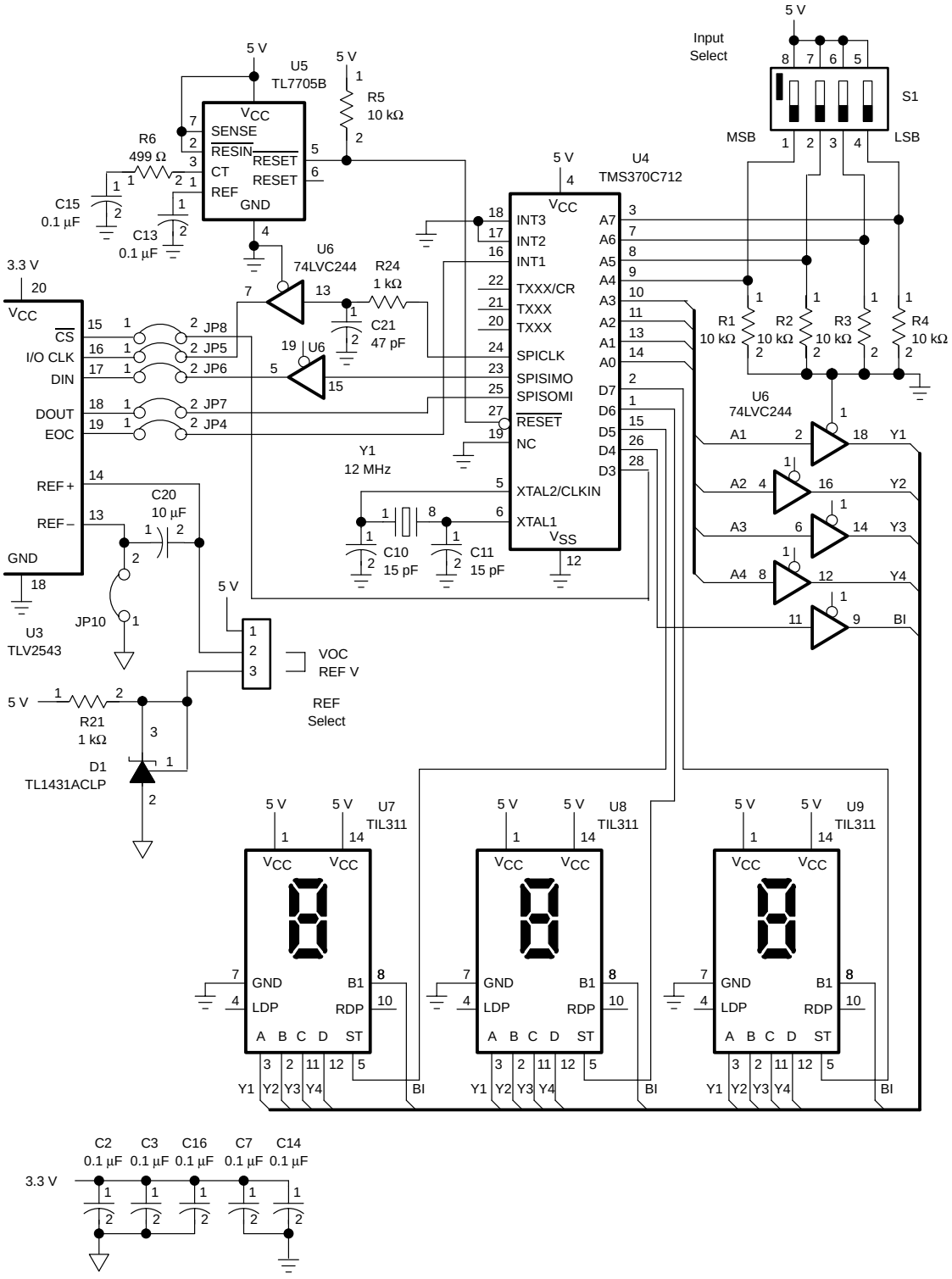


Figure 2–3 Board Schematic (continued)



2.17 Part Descriptions

A list of the TLV2543EVM parts are listed in the following table.

Table 2–5. Part Descriptions

Number	Quantity	Reference	Description
1	1	C1	100 μF, 16V Aluminum
2	14	C2, C3, C4, C5, C7, C8, C12, C13, C14, C15, C16, C17, C18, C19	0.1 μF Ceramic, Z5U, 0.2 Inch
3	2	C20	10 μF, 6.3 V Tantalum, 0.2 Inch
4	2	C9, C6	10 μF, 10 V Alum
5	2	C10, C11	15 pF Ceramic, NPO, 0.2 Inch
6	1	C21	47 pF
7	1	D1	TL1431ACLP
8	1	JP9	3 Pin Header
9	1	JP9	Shorting jumper, 2 Pin
10	1	J2	Terminal block, 2 Pos, 5 mm, side entry (OST ED1601)
11	1	Q1	2N2222A (T0-18 metal can)
12	16	R1, R2, R3, R4, R5, R10, R11, R12, R14, R15, R16, R17, R18, R19, R20	10K Ω, 1%, 0.25 W
13	1	R6	499 ΩO
14	2	R7, R8	49.9K Ω
15	1	R9	4.99K Ω
16	1	R21, R24	1K Ω
17	1	R25	1 Ω
18	1	R13	10K Ω Pot, single turn, top adj, 3/8 inch sq (Bourns 3386 P)
19	1	S1	DIP switch, 4 pos, Gold
20	1	U1	TSL250
21	1	U2	TLC2264
22	1	U3	TLV2543 (3V)
23	1	U4	TMS370C712
24	1	U5	TL7705B
25	1	U6	74LVC244A
26	3	U7, U8, U9	TIL311
27	1	U10	TPS7233Q (SOJC)
28	1	VZ1	TL7726
29	1	Y1	12 MHz crystal, HC-49/μs
30	1		PC board, TLV2543 EVM

R22, R23, C4, C5 designations unused

Chapter 3

Software Program and Flowcharts

The TLV2543EVM uses a TI TMS370C712 microcontroller to interface with the TLV2543 ADC. The program reads a four position DIP switch to determine which input is selected to be digitized. The program then uses the onboard SPI interface to communicate with the TLV2543. Sixteen bits of data (12 significant bits and 4 fill bits) are read into the processor and output on the three LED displays. This is repeated approximately every 0.5 seconds.

A fast mode can also be selected with the DIP switch. In this mode, channel four is selected as input and 20 samples are taken at about a 30 kHz rate, data is converted and displayed, and the process is repeated until another input is selected with the DIP switch. A power-down mode can also be selected which places the TLV2543 in a power-down mode and blanks the display.

This chapter includes the following topics.

Topic **Page**

3.1 Software Program

```
TMS370 Macro Assembler      Version 5.20     Thu Aug 17 17:20:54 1995
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adc_evm.asm                                                      PAGE    1

                ;;;;;;;;;;;;;;;;;;;;;;;;
                ;
                ; TLV2543 EVALUATION MODULE PROGRAM
                ;
                ;       VERSION 1.2   8/17/95
                ;
                ;       THIS PROGRAM READS A FOUR POSITION DIP
                ;       SWITCH WHICH IS USED TO SELECT THE INPUT
                ;       SIGNAL CHANNEL TO THE ADC.  THE PROGRAM
                ;       THEN SELECTS THIS CHANNEL ON THE ADC AND
                ;       CONVERTS THE ANALOG INPUT TO A 12 BIT
                ;       HEX NUMBER AND OUTPUTS THE RESULTS ON
                ;       3 7–SEGMENT DISPLAYS. POSITIONS ARE ALSO
                ;       PROVIDED TO PUT THE ADC IN A POWER DOWN
                ;     MODE AND A FAST MODE (APPROX 26 KHZ RATE).
                ;
                ;;;;;;;;;;;;;;;;;;;;;;;;
                ;;;;;;;;;;;;;;;;;;;;;;;;
                ;
                ; SYSTEM EQUATES
                ;
                ;;;;;;;;;;;;;;;;;;;;;;;;
                ;
                ; SERIAL PERIPHERAL INTERFACE (SPI) REGISTERS
                ;
        0030    SPICCR  .EQU    P030    ;SPI CONFIG REG
        0031    SPICTL  .EQU    P031    ;SPI OPERATION CONTROL REG
        0037    SPIBUF  .EQU    P037    ;SPI INPUT BUFFER
        0039    SPIDAT  .EQU    P039    ;SPI SERIAL DATA REG
        003d    SPIPC1  .EQU    P03D    ;SPI PORT CONTROL REG1
        003e    SPIPC2  .EQU    P03E    ;SPI PORT CONTROL REG2
        003f    SPIPRI  .EQU    P03F    ;SPI INTERRUPT CONTROL REG
                ;
                ; PORT A AND D REGISTERS
                ;
        0021    APORT2  .EQU    P021    ;PORT A CONTROL REG
        0022    ADATA   .EQU    P022    ;PORT A DATA
        0023    ADIR    .EQU    P023    ;PORT A DIRECTION
        002c    DPORT1  .EQU    P02C    ;PORT D CONTROL REG1
        002d    DPORT2  .EQU    P02D    ;PORT D CONTROL REG 2
        002e    DDATA   .EQU    P02E    ;PORT D DATA
        002f    DDIR    .EQU    P02F    ;PORT D DIRECTION
                ;
                ; TIMER 1 DEFINITIONS
                ;
        0040    T1CNTR1 .EQU    P040    ;MSB OF COUNTER
        0041    T1CNTR2 .EQU    P041    ;LSB OF COUNTER
        0042    TC11    .EQU    P042    ;MSB OF COMPARE REGISTER
        0043    TC12    .EQU    P043    ;LSB OF COMPARE REGISTER
        0049    T1CTL1  .EQU    P049    ;TIMER 1 CONTROL REG 1
        004a    T1CTL2  .EQU    P04A    ;TIMER 1 CONTROL REG 2
        004b    T1CTL3  .EQU    P04B    ;TIMER 1 CONTROL REG 3
                ;
                ; BIT DEFINITIONS
                ;
```

```
 56        2e        CSBIT   .DBIT   3,DDATA   ;ADC CHIP SELECT BIT
 57        31        SPIF    .DBIT   6,SPICTL  ;SPI INTR FLAF
 58        2e        DOUT1   .DBIT   5,DDATA   ;STROBE FOR DISPLAY 1
 59        2e        DOUT2   .DBIT   6,DDATA   ;STROBE FOR DISPLAY 2
 60        2e        DOUT3   .DBIT   7,DDATA   ;STROBE FOR DISPLAY 3
 61        2e        DBLANK  .DBIT   4,DDATA   ;BLANK STROBE
 62        4a        RST     .DBIT   0,T1CTL2  ;SW TIMER RESET
 63        4b        TOUT    .DBIT   5,T1CTL3  ;TIMER 1 TIME OUT
 64                  ;
 65                  ;;;;;;;;;;;;;;;;;;;;;;;
 66                  ;
 67 6000                    .TEXT   6000H   ;START OF PROGRAM
 68                  ;
 69                  ;;;;;;;;;;;;;;;;;;;;;;;
 70                  ;
 71                  ; MAIN PROGRAM
 72                  ;
 73 6000   5260      START   MOV     #60H,B
 74 6002   fd                LDSP            ;SET STACK POINTER TO 60H
 75 6003  '8e6014            CALL    INIT    ;INITIALIZE SYSTEM
 76                  ;
 77 6006  '8e6056    LOOP    CALL    READSW  ;READ INPUT DIP SWITCH
 78 6009  '8e60ed            CALL    ADC     ;DIGITIZE INPUT
 79 600c  '8e614d            CALL    DISPLAY ;DISPLAY VALUE
 80 600f  '8e6126            CALL    DELAY   ;DELAY .5 SEC
 81 6012  '00f2              JMP     LOOP
 82                  ;
 83                  ;;;;;;;;;;;;;;;;;;;;;;;
 84                  ;;;;;;;;;;;;;;;;;;;;;;;
 85                  ;
 86                  ; INIT
 87                  ;
 88                  ;       THIS ROUTINE INITIALIZES PORTS A AND
 89                  ;       D, SETS UP THE SPI, AND INITIALIZES
 90                  ;       THE DISPLAYS BY FLASHING 8 AND 0 THREE
 91                  ;       TIMES.
 92                  ;
 93 6014   f70021    INIT    MOV     #0,APORT2  ;SET PORT A TO I/O
 94 6017   f70f23            MOV     #0FH,ADIR  ;SET A4–A7=INPUT, A0–A3=OUTPUT
 95 601a   f7002c            MOV     #0,DPORT1  ;SET PORT D TO I/O
 96 601d   f7002d            MOV     #0,DPORT2
 97 6020   f7f82f            MOV     #0F8H,DDIR ;SET D3–D7 OUTPUTS
 98                  ;
 99 6023   f78030            MOV  #80H,SPICCR ;INIT SPI
100 6026   f70730            MOV  #07H,SPICCR ;SET CLOCK, 8BIT CHAR LEN
101 6029   f7033d            MOV  #03H,SPIPC1 ;SET SPI CLK TO OUTPUT
102 602c   f7223e            MOV  #22H,SPIPC2 ;SET SPISOMI AND SPISIMO TO SPI DATA
103                 ;
104 602f   720019            MOV  #0,R25      ;CLR CHANNEL REGS
105 6032   72001d            MOV  #0,R29
106                 ;
107                 ;       FLASH DISPLAY
108                 ;
109 6035   720314            MOV  #03,R20 ;SET LOOP CTR TO 3 CYCLES
110 6038   2208              MOV  #08H,A  ;SET DISPLAY REGS TO 8
```

```
111 603a   d01a             MOV     A,R26
112 603c   d01b             MOV     A,R27
113 603e   d01c             MOV     A,R28
114 6040  '8e614d    LOOP1  CALL    DISPLAY
115 6043   720218           MOV     #02H,R24 ;SET DELAY TO .5 SEC
116 6046  '8e6126           CALL    DELAY
117 6049   a4102e           SBIT1   DBLANK   ;BLANK DISPLAY
118 604c  '8e6126           CALL    DELAY
119 604f   a3ef2e           SBIT0   DBLANK   ;TURN OFF BLANK
120 6052  'da14eb           DJNZ    R20,LOOP1  ;JMP BACK IF NOT DONE
121 6055   f9        RTS
122                 ;
123                 ;;;;;;;;;;;;;;;;;;;;;;;;
124                 ;;;;;;;;;;;;;;;;;;;;;;;;
125                 ;
126                 READSW
127                 ;
128                 ;       THIS ROUTINE READS THE 4 POSITION DIP
129                 ;       SWITCH FOR THE CHANNEL NUMBER AND SAVES
130                 ;       IT IN R29.  IF 0EH IS SELECTED THE ADC
131                 ;       IS PLACED IN A POWER DOWN MODE. IF 0FH
132                 ;       IS SELECTED THE INPUT ON CHANNEL 4 IS
133                 ;       CONVERTED IN FAST MODE. ADC CHANNEL NUMBER
134                 ;       IS STORED IN R25.
135                 ;
136                 ;
137 6056   8022      READSW  MOV     ADATA,A ;READ SWITCHES
138 6058   b7                SWAP    A       ;SWAP NIBBLES
139 6059   230f              AND     #0FH,A
140 605b   1d1d              CMP     R29,A
141 605d  '0601              JNE     READ1   ;JMP IF ADC INPUT CHANGED
142 605f   f9                RTS
143                 ;
144                 ; ADC INPUT CHANGED – WAIT FOR COMPLETE
145                 ;
146 6060   d01d      READ1   MOV     A,R29   ;SAVE IT
147 6062   720318            MOV     #03,R24 ;SET DELAY FLAG TO 2 SEC
148 6065  '8e6126            CALL    DELAY
149 6068   8022              MOV     ADATA,A ;CHECK AGAIN
150 606a   b7                SWAP    A
151 606b   230f              AND     #0FH,A
152 606d   1d1d              CMP     R29,A
153 606f  '06ef              JNE     READ1
154                 ;
155                 ;SEE IF POWER DOWM MODE
156                 ;
157 6071   7d0e1d            CMP     #0EH,R29
158 6074  '061b              JNE     READ2   ;JMP IF NOT POWER DOWN
159 6076   a4102e            SBIT1   DBLANK  ;BLANK DISPLAY
160 6079   a3f72e            SBIT0   CSBIT   ;ENABLE ADC
161 607c   f70631            MOV     #06H,SPICTL
162 607f   f7ec39            MOV     #0ECH,SPIDAT
163 6082   8022      READ3   MOV     ADATA,A ;WAIT FOR CHANGE
164 6084   b7                SWAP    A
165 6085   230f              AND     #0FH,A
```

```
166 6087 * 4d001d          CMP     A,R29
167 608a  '02f6            JEQ     READ3
168 608c   a3ef2e          SBIT0   DBLANK  ;CLEAR BLANK
169 608f  '00cf            JMP     READ1
170                 ;
171                 ; SEE IF FAST MODE
172                 ;
173 6091   7d0f1d   READ2   CMP     #0FH,R29 ;IS IT FAST MODE
174 6094  '0650            JNE     READ4
175 6096   a3f72e   RLOOP1  SBIT0   CSBIT    ;ENABLE ADC
176 6099   720419          MOV     #04H,R25 ;CHANNEL 4 – FAST MODE
177 609c   224c            MOV     #4CH,A   ;CHANNEL 4,16BITS,MSB 1ST
178 609e   721414          MOV     #20,R20  ;DO 20 FAST THEN UPDATE
179 60a1   f70631          MOV     #06H,SPICTL
180 60a4   2139    RLOOP2  MOV     A,SPIDAT
181 60a6  'a74031fc RFLG1   JBIT0   SPIF,RFLG1 ;WAIT FOR DATA
182 60aa   a21537          MOV     SPIBUF,R21
183 60ad   2139            MOV     A,SPIDAT
184 60af  'a74031fc RFLG2   JBIT0   SPIF,RFLG2 ;WAIT FOR DATA
185 60b3   a21637          MOV     SPIBUF,R22
186 60b6   ff              NOP                 ;GIVE TIME FOR
187 60b7   ff              NOP                 ; CONVERSION TO
188 60b8   ff              NOP                 ;  COMPLETE
189 60b9  'da14e8          DJNZ    R20,RLOOP2
190                 ;DISPLAY VALUE
191 60bc   42151a          MOV     R21,R26
192 60bf   d71a            SWAP    R26
193 60c1   730f1a          AND     #0FH,R26   ;SAVE MSDIGIT IN R26
194 60c4   42151b          MOV     R21,R27
195 60c7   730f1b          AND     #0FH,R27   ;SAVE MIDDLE DIGIT IN R27
196 60ca   42161c          MOV     R22,R28
197 60cd   d71c            SWAP    R28
198 60cf   730f1c          AND     #0FH,R28      ;SAVE LSDIGIT IN R28
199 60d2  '8e614d          CALL    DISPLAY
200 60d5   a4082e          SBIT1   CSBIT         ;DISABLE ADC
201                 ;SEE IF FAST MODE STILL SELECTED
202 60d8   8022            MOV     ADATA,A ;WAIT FOR CHANGE
203 60da   b7              SWAP    A
204 60db   230f            AND     #0FH,A
205 60dd * 4d001d          CMP     A,R29
206 60e0  '02b4            JEQ     RLOOP1
207 60e2 *'89ff7b          JMP     READ1
208 60e5   f9              RTS
209                 ;
210                 ; SETUP CHANNEL # IN R25
211                 ;
212 60e6   421d19  READ4   MOV     R29,R25
213 60e9   720218          MOV     #02,R24  ;SET DELAY TO .5SEC
214 60ec   f9              RTS
215                 ;
216                 ;;;;;;;;;;;;;;;;;;;;;;;;
217                 ;;;;;;;;;;;;;;;;;;;;;;;;
218                 ;
219                 ; ADC
220                 ;
```

```
221                     ;       THIS ROUTINE DIGITIZES THE INPUT ON
222                     ;       THE CHANNEL SPECIFIED IN R25.  THE RESULTS
223                     ;       ARE PLACED IN REGISTERS R26, R27, AND R28.
224                     ;
225 60ed   1219        ADC     MOV     R25,A
226 60ef   b7                  SWAP    A
227 60f0   23f0                AND     #0F0H,A ;CHANNEL # IN MS NIBBLE
228 60f2   240c                OR      #0CH,A  ;16 BITS, MSB 1ST, BINARY
229 60f4   a3f72e              SBIT0   CSBIT   ;ENABLE ADC
230 60f7   f70631              MOV     #06H,SPICTL
231 60fa   2139                MOV     A,SPIDAT
232 60fc  'a74031fc    ADCFLG1 JBIT0   SPIF,ADCFLG1  ;WAIT FOR DATA
233 6100   a21537              MOV     SPIBUF,R21    ;SAVE MSBYTE
234 6103   2139                MOV     A,SPIDAT
235 6105  'a74031fc    ADCFLG2 JBIT0   SPIF,ADCFLG2  ;WAIT FOR DATA
236 6109   a21637              MOV     SPIBUF,R22    ;SAVE LSBYTE
237                     ;
238                     ; SAVE DATA
239                     ;
240 610c   42151a              MOV     R21,R26
241 610f   d71a                SWAP    R26
242 6111   730f1a              AND     #0FH,R26    ;SAVE MSDIGIT IN R26
243 6114   42151b              MOV     R21,R27
244 6117   730f1b              AND     #0FH,R27    ;SAVE MIDDLE DIGIT IN R27
245 611a   42161c              MOV     R22,R28
246 611d   d71c                SWAP    R28
247 611f   730f1c              AND     #0FH,R28      ;SAVE LSDIGIT IN R28
248 6122   a4082e              SBIT1   CSBIT         ;DISABLE ADC
249 6125   f9                  RTS
250                     ;
251                     ;;;;;;;;;;;;;;;;;;;;;;;;
252                     ;;;;;;;;;;;;;;;;;;;;;;;;
253                     ;
254                     ; DELAY
255                     ;       THIS ROUTINE USES TIMER 1 AS
256                     ;       A GENERAL PURPOSE TIMER TO
257                     ;       DELAY 0, .5, OR 2 SECONDS.
258                     ;       R24 IS SET AS FOLLOWS:
259                     ;               1=0 SEC.
260                     ;               2=.5 SEC.
261                     ;               3=2 SEC.
262                     ;
263 6126   7d0118      DELAY   CMP     #1,R24        ;SEE IF NO DELAY
264 6129  '0601                JNE     DELAY1
265 612b   f9                  RTS
266 612c   7d0218      DELAY1  CMP     #2,R24        ;SEE IF .5 SEC DELAY
267 612f  '0614                JNE     DELAY2
268 6131   f71642              MOV     #16H,TC11     ;.5 SEC COMPARE VALUE
269 6134   f7e343              MOV     #0E3H,TC12
270 6137   a40749      DLOOP   OR      #07H,T1CTL1   ;SET PRESCALER TO 256
271 613a   a4014a              OR      #1,T1CTL2     ;START COUNTER AT ZERO
272 613d   a3df4b              SBIT0   TOUT          ;CLR CMP FLAG
273 6140  'a7204bfc    DFLAG1  JBIT0   TOUT,DFLAG1   ;WAIT FOR TIMEOUT
274 6144   f9                  RTS
275 6145   f75b42      DELAY2  MOV     #5BH,TC11     ;2 SEC COMPARE VALUE
```

```
276 6148   f78d43            MOV     #8DH,TC12
277 614b  '00ea              JMP     DLOOP
278                  ;
279                  ;;;;;;;;;;;;;;;;;;;;;;;;
280                  ;;;;;;;;;;;;;;;;;;;;;;;;
281                  ;
282                  ; DISPLAY
283                  ;
284                  ;       THIS ROUTINE DISPLAYS THE HEX
285                  ;       DIGITS STORED IN REGS R26, R27,
286                  ;       AND R28.
287                  ;
288 614d   321a      DISPLAY MOV     R26,B       ;OUTPUT LSD
289 614f  'aa6175           MOV     *DTBL[B],A
290 6152   2122             MOV     A,ADATA
291 6154   a3df2e           SBIT0   DOUT1       ;STROBE IT
292 6157   a4202e           SBIT1   DOUT1
293 615a   321b             MOV     R27,B       ;OUTPUT MIDDLE DIGIT
294 615c  'aa6175           MOV     *DTBL[B],A
295 615f   2122             MOV     A,ADATA
296 6161   a3bf2e           SBIT0   DOUT2
297 6164   a4402e           SBIT1   DOUT2
298 6167   321c             MOV     R28,B       ;OUTPUT MSD
299 6169  'aa6175           MOV     *DTBL[B],A
300 616c   2122             MOV     A,ADATA
301 616e   a37f2e           SBIT0   DOUT3
302 6171   a4802e           SBIT1   DOUT3
303 6174   f9               RTS
304 6175   00        DTBL    .BYTE   00H     ;0
305 6176   08                .BYTE   08H     ;1
306 6177   04                .BYTE   04H     ;2
307 6178   0c                .BYTE   0CH     ;3
308 6179   02                .BYTE   02H     ;4
309 617a   0a                .BYTE   0AH     ;5
310 617b   06                .BYTE   06H     ;6
311 617c   0e                .BYTE   0EH     ;7
312 617d   01                .BYTE   01H     ;8
313 617e   09                .BYTE   09H     ;9
314 617f   05                .BYTE   05H     ;A
315 6180   0d                .BYTE   0DH     ;B
316 6181   03                .BYTE   03H     ;C
317 6182   0b                .BYTE   0BH     ;D
318 6183   07                .BYTE   07H     ;E
319 6184   0f                .BYTE   0FH     ;F
320                  ;;;;;;;;;;;;;;;;;;;;;;;;
321                  ;;;;;;;;;;;;;;;;;;;;;;;;
322 7ffe                     .SECT   "RESET",7FFEH   ;RESET VECTOR ADDR
323 7ffe   6000              .WORD   6000H   ;PROGRAM START
324                  ;
325                          .END

 No Errors,  No Warnings
```

3.2 Flowcharts

The flowcharts for the TLV2543EVM are shown in the following figures.

Figure 3–1. Main Program Flowchart

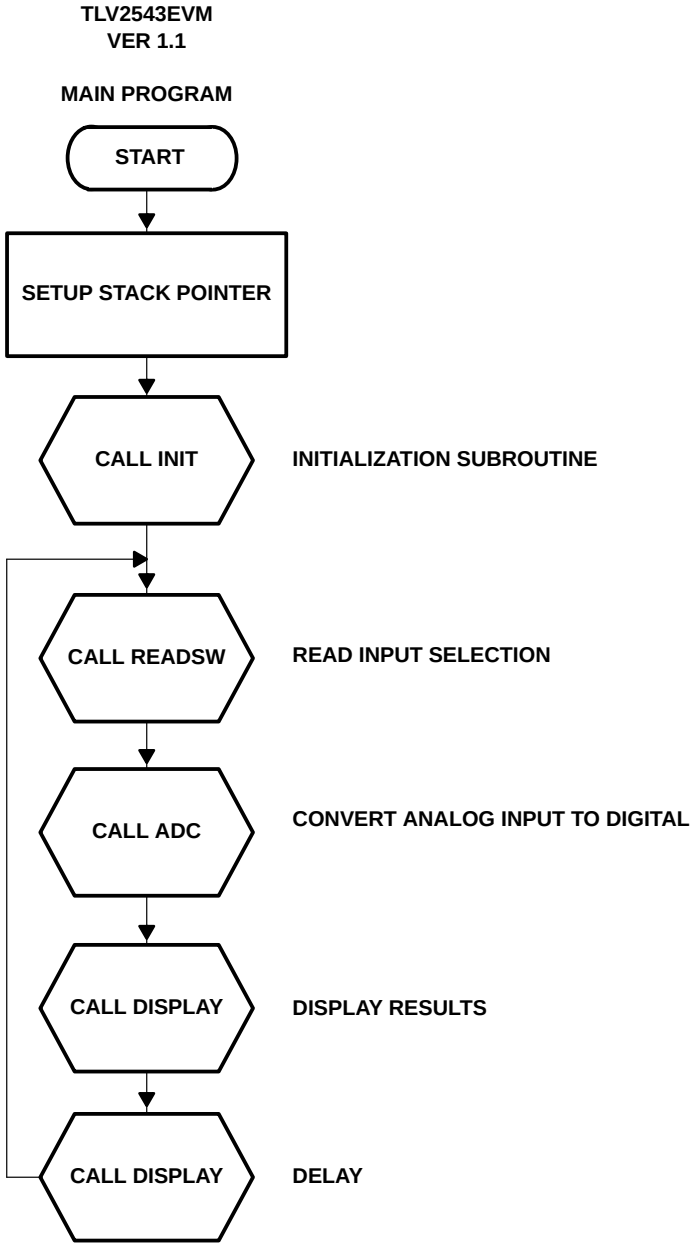

Figure 3–2. Initialization Subroutine Flowchart

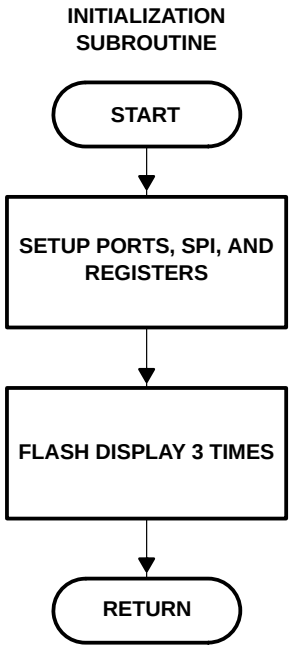

Figure 3–3. Read Input Switch Subroutine Flowchart

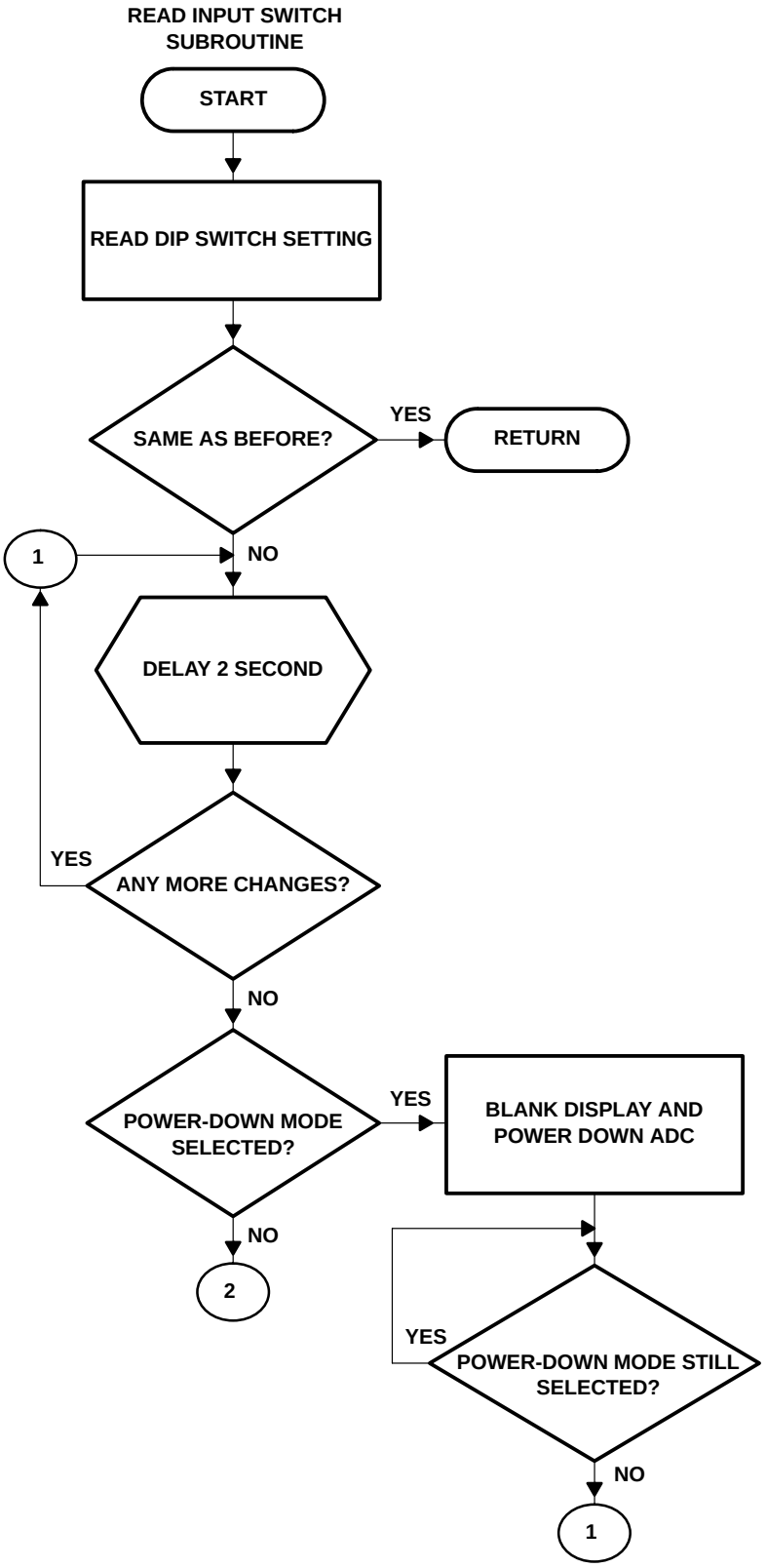

Figure 3–3 Read Input Switch Subroutine Flowchart (continued)

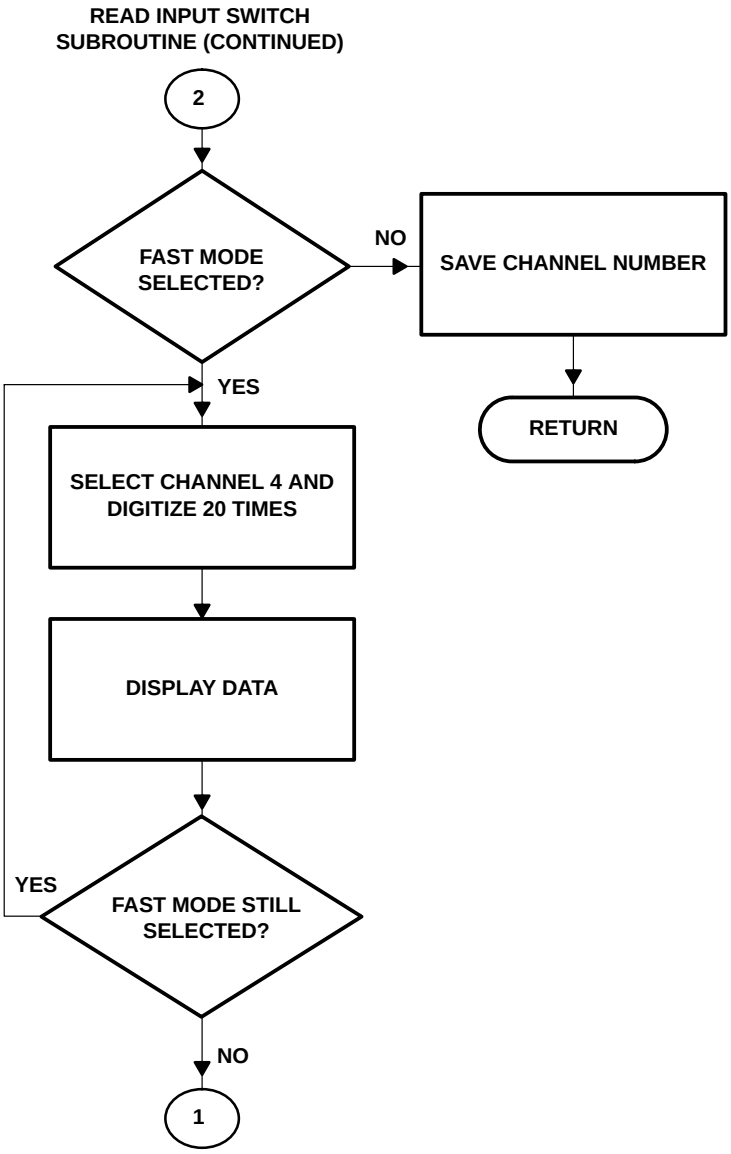

Figure 3–4. Analog-to-Digital Convert Subroutine Flowchart

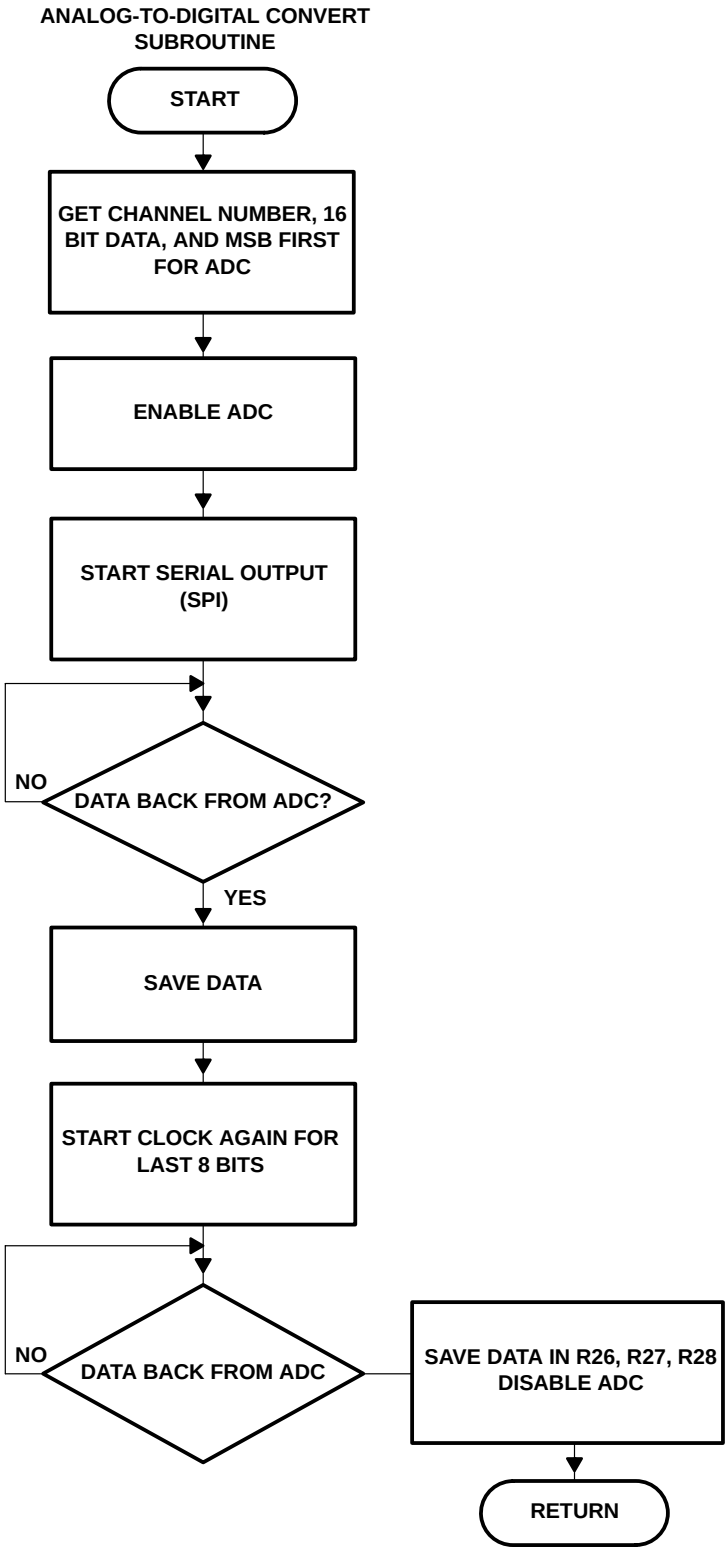

Figure 3–5. Delay Subroutine Flowchart

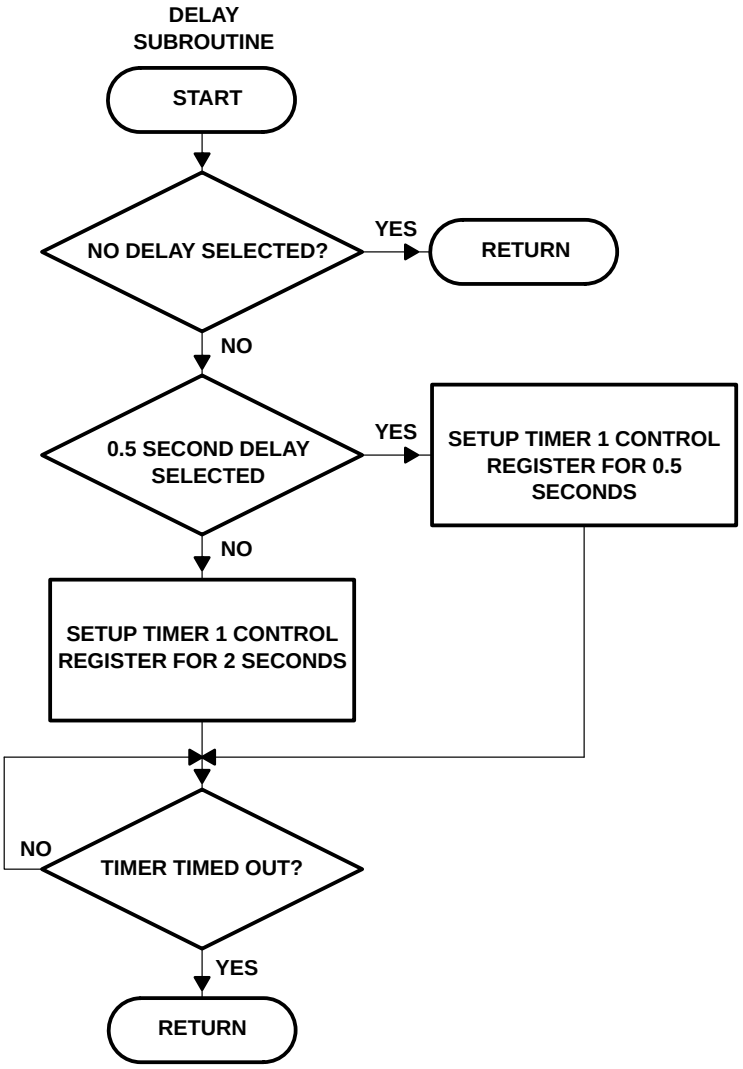

Figure 3–6. Display Subroutine Flowchart